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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,175	DANG ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007 and 10 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-14 and 16-26* is/are rejected.

7)☐ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment 6/22/2007 and RCE dated 7/10/2007.

The applicant has canceled claims 1, 8 and 15.

The applicant has amended claims 2, 4, 9, 11, 16, 18-26.

Claims 2-7, 9-14 and 16-26 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/22/2007 has been entered.

Response to Amendment

2. As per the objections to the drawings (item 6 of office action dated 4/11/2007), the applicant's argument is unpersuasive. The applicant has admitted (Remarks, page 8, 2nd and 3rd paragraphs) that "the output of register 455 is coupled to an input of the multiplexer 460 via AND gate 475" (examiner underlined). Since the claims are the legal description of the invention, it is important that the limitations be clear. But it is clear to anyone of ordinary skill that the "couplings" cited in the claims 22, 24 and 26 are direct

couplings. Please note that all of the other "couplings" cited by the applicant in claims 21, 22, 23, 24, 25 and 26 which are not objected to, are indeed direct couplings! It must be assumed therefore that in view of all other couplings being direct, the "couplings" at issue by the examiner in the previous office action must also be direct, and so the drawings are maintained as being objected to because the drawings do not illustrate the claims 22, 24 and 26.

3. As per the rejections under 35 USC 112 first paragraph (item 7 of office action dated 4/11/2007) of claims 22, 24 and 26, the applicant's argument is unpersuasive. The applicant argues that "coupled" is not a *direct connection*. But the definitions of each word are very closely related, where, for instance, in the on-line dictionary Google (http://www.google.com/search?hl=en&lr=&as_qdr=all&defl=en&q=define:coupled&sa=X&oi=glossary_definition&ct=title), the word "coupled" means "connected by a link" (examiner underlined). It would therefore follow that if the two words "connected" and "coupled" are used in the same definition, *the words must be similar*. The coupling being applied to the rejected claims, with a coupling between the register output and the multiplexer input therefore has not been disclosed in the original specification. Therefore the examiner maintains the rejection based on the usage of the word "coupled" as being a "connection".

4. In view of the applicant's cancelling of independent claims 1, 8 and 15, all rejections of said claims under 35 USC 103 are withdrawn, as well as the rejections of

the dependent claims under 35 USC 103 thereof. Applicant's arguments with respect to claims 2-7, 9-14 and 16-26 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Objections (New)

5. Claim 24 is objected to because of the following informalities: In order to leave no doubt that the instructions are *embodied in* the storage medium, the examiner requests that line 2 of the claim 24 be amended to recite, "... a set of instructions ~~adapted~~ therein to ~~operate~~ cause an information ...". Appropriate correction is required.

Claim Rejections - 35 USC § 112 (New)

6. Claims 22 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Each claim cites three instances of an antecedence issue wherein each claim 22 and 26 recites the limitations "at least one input register" in line 4, "an input" in line 4, and "an output of a multiplexer" in lines 4 and 5 respectively. Each of the herein quoted limitations has already been cited in the preceding claims 21 and 25, and so it is unclear what the applicant intends to claim. For instance, are the quoted limitations in claims 22 and 26 new instantiations of new limitations, or are the quoted limitations the same ones as were cited in the previous claims?

Claim Rejections - 35 USC § 103 (New)

7. Claims 2-3, 16-17, 19-21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6996758, and further in view of Jin, U.S. Patent No. 6114892.

As per claims 21 and 25:

Herron teaches a method based on a reconfigurable device for testing a set of interface connections in the reconfigurable device (see Title) between an IP core implementing at least one specialized operation and a set of functional blocks (column 3 lines 34-40) adapted to implement general-purpose logic devices (see Abstract), the method comprising: creating a test program including a set of test data and a test configuration adapted to configure the set of functional blocks (column 1 lines 51-60 and column 2 lines 14-25) to implement a set of boundary scan registers (column 23 lines 30-32) connected with the interface connections of the IP core (see FIG. 27); configuring the reconfigurable device according to the test configuration (column 3 lines 57-67); inputting the test data into the reconfigurable device (for example, column 2 lines 58-67) to create a set of test results (column 3 lines 1-15); and analyzing the set of test results to determine the integrity of the set of interface connections (column 3 lines 34-40), and wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers (see FIG. 27), the set of boundary scan registers including at least one input register (FIG. 27), but where Herron only illustrates generic input and output scan registers without specific wiring, the analogous art of Jin further discloses

the input register (see FIG. 3 220, FIG. 4 224 and FIG. 7 270 for example) having an input (the D input) coupled to an output of a multiplexer (output of FIG. 4 226), and an output (FIG. 3/4 Q') coupled to a first input of a logic gate (FIG. 3 output 210 coupled to gate 214), where a select input for the multiplexer (FIG. 3 SE) is coupled to a second input of the logic gate (FIG. 3 SE at 210 connected to 2nd input of 214) and an output of the logic gate (FIG. 3 Q) is coupled to an input of the IP core (FIG. 7 220 Q coupled to logic 230). And in the Abstract, the advantage stated is a scan chain device that may be of low power, yet less noisy during scan mode testing. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the features of Jin to the scan chain of Herron, including wiring of FIG. 3, in order to better control the noise in the test circuits while scanning data.

As per claim 2:

Herron further teaches the method of claim 21, wherein the set of boundary scan registers include a plurality of shift registers connected in series (column 15 lines 50-62), wherein each shift register is adapted to be connected with an interface connection of the IP core (column 15 lines 50-62 as applied to FIG. 27). And in view of the motivation previously stated, the claim is rejected.

As per claim 3:

Herron further teaches the method of claim 2, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core (FIG. 27 2702 and column 18 lines 14-20) and a second portion of the plurality of shift registers is adapted to be connected with a set of output

interface connections (FIG. 27 2708 and column 18 lines 28-34) of the IP core (FIG. 27 2704 column 17 lines 65-67 and column 18 lines 1-13). And in view of the motivation previously stated, the claim is rejected.

As per claim 16:

Herron further teaches the information storage medium of claim 25, wherein the set of boundary scan registers include a plurality of shift registers connected in series (column 15 lines 50-62), wherein each shift register is adapted to be connected with an interface connection of the IP core (column 15 lines 50-62 as applied to FIG. 27). And in view of the motivation previously stated, the claim is rejected.

As per claim 17:

Herron further teaches the information storage medium of claim 16, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core (FIG. 27 2702 and column 18 lines 14-20) and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections (FIG. 27 2708 and column 18 lines 28-34) of the IP core (FIG. 27 2704 column 17 lines 65-67 and column 18 lines 1-13). And in view of the motivation previously stated, the claim is rejected.

As per claim 19:

Herron further teaches the information storage medium of claim 25, further including a set of test data adapted to be input into the IP core via the set of functional blocks implementing the set of boundary scan registers (see Abstract). And in view of the motivation previously stated, the claim is rejected.

As per claim 20:

Herron further teaches the information storage medium of claim 25, further including a set of expected test results (column 4 lines 24-32). And in view of the motivation previously stated, the claim is rejected.

8. Claims 4-7, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al. (herein Herron), U.S. Patent No. 6996758, in view of Jin, U.S. Patent No. 6114892 as applied to claims 21 and 25 above, and further in view of Kiryu et al. (herein Kiryu), U.S. Patent Application Publication No. 2005/0138509.

As per claims 4, and 18:

Where Herron and Jin fail to further teach, Kiryu discloses the method/device of claim 21 or 25, wherein the test configuration is defined with a hardware description language representation (see the Background of Kiryu). And in the Background, the advantage stated was that for scan chain testing used in design verification, testing a design within scan chains, and verifying functionality of a design, is expedited with the use of HDL. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply a modern test aid such as HDL as cited in Kiryu, in the design and test stages of a circuit using scan chains such as in Herron in order to test the device.

As per claims 5:

Kiryu further teaches the method of claim 4, wherein the creating a test program includes: combining the hardware description language representation of the test

configuration with a hardware description language representation of the IP core to form a test hardware description; and analyzing the test hardware description to create a set of test data. Kiryu, in the Background describes such a process for both scan chains and the embedded logic. And in view of the motivation previously stated, the claims are rejected.

As per claims 6:

Herron further discloses the method of claim 5, wherein creating a test program further includes analyzing the test hardware description and the set of test data to create a set of expected test results; and wherein analyzing the test results includes comparing the set of test results with the set of expected test results (column 2 lines 58-67 and column 3 lines 1-3). And in view of the motivation previously stated, the claims are rejected.

As per claims 7:

Herron further suggests the method of claim 5, wherein analyzing the test hardware description is performed using automated test program generation software. The disclosure, in column 3 lines 16-26) states that during the test vector generation, "known test procedures" are applied in generating test vectors. Support for such a well known process in the art using ATPG may be found in analogous references such as by Renovell, "IS-FPGA: A New Symmetric FPGA Architecture with Implicit SCAN", November 1, 2001, IEEE International Test Conference 2001, page 930, column 2, 2nd paragraph. And in view of the motivation previously stated, the claims are rejected.

9. Claim 24 and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6996758, and further in view of Suzumura, US Patent No. 7058867.

As per claim 24:

Herron teaches an information storage medium including a set of instructions adapted to operate an information processing device to perform a set of method steps, the set of steps comprising: creating a test program including a set of test data and a test configuration adapted to configure the set of functional blocks (column 1 lines 51-60 and column 2 lines 14-25) to implement a set of boundary scan registers (column 23 lines 30-32) connected with interface connections of an IP core (see FIG. 27); configuring the reconfigurable device according to the test configuration (column 3 lines 57-67); inputting the test data into the reconfigurable device (for example, column 2 lines 58-67) to create a set of test results (column 3 lines 1-15); and analyzing the set of test results to determine the integrity of the set of interface connections (column 3 lines 34-40), and wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers (see FIG. 27), the set of boundary scan registers including at least one input register (FIG. 27), but where Herron only illustrates generic input and output scan registers without specific wiring, the analogous art of Suzumura further discloses including at least one input register (see FIG. 1 21a), the input register having an input (the D input) coupled to an output of a multiplexer(FIG. 1 22a) and an output (the Q~ output) coupled to an input of the multiplexer (see FIG. 1). And in column 3

lines 6-60, the advantage stated was a better way to exercise circuits during stress testing by alternating the polarity of the test data more efficiently with the wiring of FIG. 1. One of ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to implement the feedback of shift registers as in Suzumura into the test system of Herron in order to include the improved stress test method.

As per claim 9:

Herron further teaches the method of claim 24, wherein the set of boundary scan registers include a plurality of shift registers connected in series (column 15 lines 50-62), wherein each shift register is adapted to be connected with an interface connection of the IP core (column 15 lines 50-62 as applied to FIG. 27). And in view of the motivation previously stated, the claim is rejected.

As per claim 10:

Herron further teaches the method of claim 9, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core (FIG. 27 2702 and column 18 lines 14-20) and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections (FIG. 27 2708 and column 18 lines 28-34) of the IP core (FIG. 27 2704 column 17 lines 65-67 and column 18 lines 1-13). And in view of the motivation previously stated, the claim is rejected.

As per claim 11:

Where Herron fails to further teach, Kiryu discloses the method of claim 24, wherein the test configuration is defined with a hardware description language

representation (see the Background of Kiryu). And in the Background, the advantage stated was that for scan chain testing used in design verification, testing a design within scan chains, and verifying functionality of a design, is expedited with the use of HDL. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply a modern test aid such as HDL as cited in Kiryu, in the design and test stages of a circuit using scan chains such as in Herron in order to test the device. And in view of the motivation previously stated, the claim is rejected.

As per claim 12:

Kiryu further teaches the method of claim 11, wherein the creating a test program includes: combining the hardware description language representation of the test configuration with a hardware description language representation of the IP core to form a test hardware description; and analyzing the test hardware description to create a set of test data. Kiryu, in the Background describes such a process for both scan chains and the embedded logic. And in view of the motivation previously stated, the claims are rejected.

As per claim 13:

Herron further discloses the method of claim 12, wherein creating a test program further includes analyzing the test hardware description and the set of test data to create a set of expected test results; and wherein analyzing the test results includes comparing the set of test results with the set of expected test results (column 2 lines 58-67 and column 3 lines 1-3). And in view of the motivation previously stated, the claims are rejected.

As per claim 14:

Herron further suggests the method of claim 12, wherein analyzing the test hardware description is performed using automated test program generation software. The disclosure, in column 3 lines 16-26) states that during the test vector generation, "known test procedures" are applied in generating test vectors. Support for such a well known process in the art using ATPG may be found in analogous references such as by Renovell, "IS-FPGA: A New Symmetric FPGA Architecture with Implicit SCAN", November 1, 2001, IEEE International Test Conference 2001, page 930, column 2, 2nd paragraph. And in view of the motivation previously stated, the claims are rejected.

10. Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6996758, and further in view of Jin, U.S. Patent No. 6114892 as applied to claims 21 and 25 above, and further in view of Suzumura, US Patent No. 7058867.

As per claims 22 and 26:

Where Herron and Jin have failed to specifically disclose, the analogous art of Suzumura further teaches the method and reconfigurable device of claims 21 and 25 wherein the set of boundary scan registers include at least one input register (see FIG. 1 21a), the input register having an input (the D input) coupled to an output of a multiplexer (FIG. 1 22a) and an output (the Q~ output) coupled to an input of the multiplexer (see FIG. 1). And in view of the motivation previously stated, the claims are rejected.

11. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al., (herein Herron), U.S. Patent No. 6996758, in view of Suzumura, US Patent No. 7058867 as applied to claim 24 above, and further in view of Jin, U.S. Patent No. 6114892

As per claim 23:

Where Herron and Suzumura have failed to specifically disclose, the analogous art of Jin further teaches the information storage medium of claim 24 wherein the set of boundary scan registers include at least one input register, the input register (see FIG. 3 220, FIG. 4 224 and FIG. 7 270 for example) having an input (the D input) coupled to an output of a multiplexer (output of FIG. 4 226), and an output (FIG. 3/4 Q') coupled to a first input of a logic gate (FIG. 3 output 210 coupled to gate 214), where a select input for the multiplexer (FIG. 3 SE) is coupled to a second input of the logic gate (FIG. 3 SE at 210 connected to 2nd input of 214) and an output of the logic gate (FIG. 3 Q) is coupled to an input of the IP core (FIG. 7 220 Q coupled to logic 230). And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John P Trimmings/
Examiner, Art Unit 2117
01/17/2008

jpt